

# DESTA TADESSE

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## EDUCATION

### **Brown University**, Providence, RI

- PhD Student in Electrical Sciences and Computer Engineering
- MSc. Engineering (Electrical sciences and CE), *May 2006*

*August 2004 – present*

#### Relevant Coursework:

Design and Implementation of VLSI Systems

Digital Signal Processing

Timing Analysis tool design (CAD independent study)

Introduction to Semiconductor Electronics

Digital Integrated Circuit Testing

Advanced Computer Architecture

### **Connecticut College**, New London, CT

- B.A in Computer Science, *summa cum laude*, *May 2004*
- B.A in Physics, *summa cum laude*, *May 2004*

#### Relevant Coursework:

Digital Electronic Design

Advanced Programming Languages

Algorithms

Networks

Programming Data Structures

Electromagnetic Theory

## AWARDS AND HONORS

Brown Graduate Fellowship *2004*, Phi Beta Kappa *2004*, Sigma Pi Sigma (National Physics Honor Society) *2003*, Keck Grant Award *2001–2002*, Julia Wells Bower Prize for outstanding achievement in mathematics *2002*, Connecticut College Academic Scholarship *2000*, Presidential Award for excellence in academics *2000*

## RESEARCH EXPERIENCE

### **Intel Graduate Intern**, EMG, MMDC, Intel Massachusetts, Hudson, MA

*August 2006 – Jan 2007*

- Developed and wrote tools (C++/Perl) needed for post-silicon debug of a next-technology Itanium processor. One specific tool was focused on automating the best way to configure certain devices during post-Si to allow for debug and speed push efforts. This was done using decision solvers.
- Improved and validated algorithms for a tool that configures and manipulates on-die debug devices to run faster and more robustly
- Conducted experiments on IMS vanguard testers to test the efficiency of algorithms.
- Wrote scripts to process and analyze data from large-unit experiments to characterize chips.
- Presented my work to my group frequently.

### **Research Assistant**, Brown University, Providence, RI

*Sept 2003 – Present*

- Develop accurate timing analysis tools capable of handling the effects of multiple inputs switching. In particular, the approach is to unroll the circuit in time and pose timing questions as decision problems to a SAT solver. General area of interest is primarily in the area of CAD for VLSI systems, in particular, timing analysis and verification tools.

### **Research Associate**, Ammerman Center for Arts and Technology, New London, CT

*June 2003 – May 2004*

- Explored the potential of using Xilinx DSP boards as hardware to design and implement custom processors that rival dedicated DSP processors for speed and efficiency.

### **Researcher**, Dhaglian Ion Accelerator Lab, New London, CT

*June 2001 – May 2004*

- Responsibilities included designing and building complete optics system for the accelerator target chamber, aiding in the design of the complete target chamber, setting up and implementing software to control the process of capturing spectroscopic images, and supervising and training other students in the operation of the particle accelerator.

## PUBLICATIONS

- Desta Tadesse, Michael Black, Iris Bahar, Joel Grodstein. *Accurate Timing Analysis using SAT and Pattern-Dependent Delay Models*. Design Automation and Test in Europe (DATE), 2007.
- Tom Ammirati, Michael Monce, Desta Tadesse, Peter Luthy. *Absolute photon cross sections for Balmer lines from proton-SO<sub>2</sub> collisions*. Journal of Geophysical Research, Vol. 110, A04214, 2005.

## PRESENTATIONS

- *Accurate SAT-based Timing Analysis: Theory and Implementation*. Series of bi-monthly status reports to Intel CAD and verification engineers updating on the progress of my current research project and discussing potential problems and solutions, 2004 – 2006.
- Tom Ammirati, Desta Tadesse, Michael Monce. *Photon Emission Spectrum and Cross Sections of  $He^+ + SO_2$* , CAARI 2004, Denton, TX.
- Tom Ammirati, Michael Monce, Desta Tadesse. *Absolute Photon Emission Cross Sections for Balmer Lines from Proton-SO2 Collisions*, CAARI 2002, Denton, TX.

## SKILLS OVERVIEW

**Programming Languages:** C++, Java, C, Perl, ML, Verilog, UNIX and Windows OS

**CAD:** Matlab, Silvaco SmartSpice, Tanner EDA, SIS, SimpleScalar

**Chip Tester:** IMS Vanguard

**Languages:** Fluent in English and Amharic, proficient in French

## TEACHING EXPERIENCE

**Teaching Assistant**, Brown University, Providence, RI

*Spring 2005, Fall 2005&2007*

- Assisted in the instruction of senior level courses on *computer architecture* and *digital electronic systems design*. Responsibilities included grading, setting up labs, assisting students with labs and homework, and giving class lectures during instructor's absence.

**Teaching Assistant**, Connecticut College, New London, CT

*2003 – 2004*

- Assisted in the instruction of courses such as *Calculus I*, *Discrete Mathematics* and *Intro to Physics*. Responsibilities included grading, setting up labs, assisting students with labs and homework, and holding recitation sections.

## INTERESTS

Soccer and Salsa