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EN291 NANOSYSTEM DESIGN

Nano-wire Based Programmable Architectures

The presentation of Mickey was primarily based on nanowire architectures, how to make NWs physically in terms of the steps that are involved in the NW growing process ,why nanowires are important for today's circuit's designs as: FET and diodes, etc. and how we get using the nanowires in various applications such as memory, programmable wired plane's blocks, decoders, logic circuits, nanoPLA blocks .we have agreed that nanowire is a important architecture to build NanoBlock for the universal nanocomputing machine in the future.

Advantageous of Nanowires:

One of the most important advantageous of the nanowires is that they are very small and they are more uniform compared to the nanotubes because we do not know how to selectively synthesize CNTs with particular properties ,differentiate CNTs along their length as we do with Nanowire, and alignment CNTs into straight for building arrays. Nanowires are built or fabricated easier than NanoTubes and they are more convenient investment in both time and money.

Technology & Growing Nanowires:

One way to make a nanowire is chemical etching process which takes a bigger wire and etches the unnecessary parts in order to get a wire in nano size. But Mickey argued that this process is not used in the today's applications rather it remained only in theory. Besides chemical etching process the bigger wires can also be bombarded with energetic particles so that at the end of the process nanowires are formed from bigger wires. The last method that Mickey had mentioned was Vapor Liquid Solid synthesis method. In order to able to grow semiconductor nanowires with this method seed catalysts are used (Gold (Au) is one of the possibilities which is specific to the nanowires) and with using the seed catalysts the nanowires' diameters are defined. (diameter with 3nm can be formed) Hence the diameter of the nanowire is closely related to the diameter of seed catalysts. One possible problem at this point is as nanowires get smaller and smaller the edge effect becomes more and more. So the edge effect is a defect for nanowires and their ability of conducting electricity will diminish due to this edge effect. After having a basic idea of how to make nanowires the coming next part will show how to adjust NWs electrical properties and conductivity. Basically there are two options for controlling doping profile or material composition along a NW.

*Axial Profile: is one way to adjust the conductivity of NW's. The doping profile is controlled by variable material concentrations during the time when NWs are grown. One of the most important aspects of this type of a control is no lithography process is required for controlling the physical dimensions.

*Radial Profile: is another way to control doping profile or material composition by changing the radius of the Nws. By adding layers along entire surface we can adjust the doping profile.
Since adding the more length of Nanowire, the more opportunity in making Nanowire's bended and broken. Consequently we should limit NW lengths like 10 microns for building good nanowire arrays.

WHY ADDING LAYERS ?

NWs are very close to each other and by insulating them properly you can compact the NWs even more closely. So an answer to this question is then we have to add layers in order insulate them. One of the most interesting aspects of building an insulating layer is that you are building the insulating layer without having a new material or new composition rather by adjusting the temperature and pressure you can build an insulating layer. SiO2 is used for insulating layers between NWs. And also you can have different addressing on nanowires. The each layer can be etched properly so that you will get different addressing schemes for each nanowire at the end.

Electrical Properties of NWs:
The physical properties of nanowires and Silicon are same. They have good on/off resistance, they have doping and FET properties, their threshold can be controlled via changing the geometry or material properties.

APPLICATIONS
As we all know that the fact nanowires can be used as more than just interconnect wires, rather they can be used as active devices.

HETEROGENOUS NW: When junctions are created in NWs the steps are based on how many junctions you want to implement in NW. After having first reactant and creating one type of junction lets say A-type junction the second reactant has to be put in order to create another junction say B-type junction and these steps can be repeated based on the choice of junctions' numbers in the NW. A discussion was followed at this step about the possible problems of these junctions which is one material can leak to another because of the gap between two materials. Because the junctions are not well defined the region between the junctions are not sharp which could prevent the proper operation of the junctions and diminish the reliability.

NW-FET: Chemical Vapor Deposition or Dopant modulation is a way for fabricating p-n junction Nws Then p-n junction NWs can be used as building blocks for FETs. NW-FETs consist of only from one nanowire and one contact so it can't be used that much but it is a still good first attempt for studying their properties. From the I-V curve it can be understood that their functionality is like p-n junction which n type acts like a gate whereas p-type acts as a channel.

NW-DIODE: Two semiconductor NWs, one p-type and one n-type, form a junction diode at their crossing. Three NWs with two crossings form a bipolar junction transistor. Small working NW diode arrays can be made, with 85% to 95% yield. Turn-on voltages of IV are observed, and logic gates may be made with crossed nanowire diodes. NW-diodes consist of two nanowires that can be formed into a PN junction whose current rectifying characteristics are the same as p-n diodes. The electrical properties and the functionality of these junctions can also be controlled. Low or high turn-on voltage devices can be made by changing the oxide thickness and junction between two nanowires. This oxide can be grown by passing high current through a low turn-on diode in air, oxidizing the junction by joule heating.

cNW_FET: (crossed NW-FETs) CNW-diodes act as FETs in their non-conducting region. A p channel crossed nanowire FET (CNW-FET) has a p-type single crystal silicon NW channel and n-type single-crystal gallium nitride NWgates. cNW-FETs enable us to form more complex logic gates. Nanowires are arranged into crossbar arrays and each cross point between crossed wires can store its own information.From the I-V graph it can concluded that there is a large decrease in conductance by an increase in the gate voltage. One of the most important aspects of the cNW-FETs are that they are reproducible and repredictable and they can be easily integrated to logic gates.

From the information for Nanowire applications we can see the difference between NW-diodes and NW-FETs clearly that NW-diodes operate as two terminal devices wherea NW-FETs operate as three terminal devices.

LOGIC USING NW-FET:

One of the most challenging parts of logic design is contacts. The usage of the contacts for this integration process makes the design bigger because since NWs are integrated on CMOS subsystem. Basically contacts take up whole space that you are gaining with NWs. Examples for NW-FET based logic structures were talked in class after having some background about how a diode works in principle. NOR and AND gate examples were talked in the class. The OR gate is constructed from “2(p-Si) by 1(n-GaN) crossed p-n junction”, called NW-diode, 2-terminal device. Also the AND gate is constructed from p-n crossed junction array but with 1(p-Si) by 3(n-GaN). Whereas, the NOR gate is constructed from “1(p-Si) by 3(n-GaN) crossed NW-FET”, 3-terminal device.

NOR GATE: In order to create an NOR gate 2 p Si and 1n GaN should be crossed on a p-n array. The two p-Si are inputs and the one n-GaN NW is the output. The connection is made such that the diodes that are formed are conducting the current when one of the inputs or both of the inputs are at logic high level. Meaning that given one of the inputs or both of them are at high voltage the diodes will be operating in forward biased mode allowing a current flow so at the output logic high can be observed. Whereas when both of the inputs are at logic low level both of the diodes will operate in reverse biased meaning no current flow and output voltage will be zero. Since the AND gate formation was more challenging Professor Bahar asked Mickey to go over AND gate example.

AND GATE: The AND gate formation from NW-FETs was more challenging than NOR. The two of the GaN NWs are inputs, while the third one is used for depleting a portion of the p-Si NW, biased at 5V, with a constant voltage in order to create a resistor. Two NW-FETs are connected to output via a resistance reversely. So then applying 0 0 for the inputs will make both of the diodes in forward biased operation and they begin to conduct current so output voltage will be lowered through the resistance and goes to zero and for applying 1 1 for each input make the diodes to operate in reverse biased region where they do not conduct current and output voltage remains at its high voltage value. At this point Dimitri made a point by saying that then we have to give a value for the output first so for example for 0 0 case it can be lowered from high voltage which was refused by the argument that output can also go to zero from a n unknown value x.

ASSEMBLY & CROSSPOINTS:

How to order the NWs?

With assembly techniques we can build regular NW arrays meaning a set of NWs can be aligned into a single orientation. The cross-points can't be different from other ones due to the small size of them, for example,10nm cross point size is so small that it can't be differentiated from another one. Mickey's interpretation for this regular assembly was in a a negative way by saying that “they are so regular that you can't make one cross point different than another” whereas Professor Bahar refused Mickey's interpretation by pointing the advantages of having standard regular structures. One counter example for this issue was made by Mickey about creating different characteristics. For example when you are making a CMOS design you can change your drive strength by altering width of the transistor whereas you can't do this with nanowires.

CHALLENGES:

Fabrication: Perhaps the largest difference between molecular electronics and traditional VLSI is in the methods of fabrication. Molecular electronics is based on bottom-up manufacturing as opposed to the traditional top-down approaches used in manufacturing today’s chips. Bottom-up manufacturing is of necessity a hierarchical process. First the individual devices and wires are manufactured. Then individual devices must be assembled into systems for device and circuit experiments. To create successful molecular electronics systems we must be able to assemble the individual components into larger subunits. These subunits would then be connected together into complete systems.

- bottom-up approach: Getting closer and closer to atomic scale the top-down approach of the conventional lithography process becomes harder to maintain and repeatability becomes another issue. So the bottom-up approach has to be used but there are some disadvantages of this approach in terms of non-perfect and deterministic alignment in three dimensions.
- Regular assembly (?? questioned in the class about what is wrong having regular structures.)
- NWs are not too long or not too tall. This is ok when you are designing logic circuits but for memory structures that would be a problem.
- Contact issue between two NWs or between a NW and a metal connection
- decoder algorithm for connecting the nanowires to outside world.

For nanoscale circuits, another challenge is to design components simple enough to fabricate by self-assembly that are nevertheless useful for constructing complex circuits. Arrays of parallel nanowires, microns long with nanometer pitch, are one such example. Two of these arrays, placed orthogonally with molecules between the crossed wires, can be configured to provide electronic memory and logic circuits. Configuring and using these circuits requires electrical connections to standard microelectronics so that the nanowires are individually addressable.

BUILDING BLOCKS

After having the knowledge about how to assembly NWs the building blocks can be made and with the help of these building blocks programmable architectures can be constructed.

MEMORY CORE:

With the help of the assembly process NWs can be created into arrays which can serve as memory cores. Applying voltage accross a cross point junction the cross point will be in either high or low resistance stage. Having a voltage source on columns and rows a cross point can be set uniquely to a high voltage or low voltage. If you want a read data you have to apply a test voltage to a column and then observe the current flow to read the cross point state.

ADRESSING NANOWIRES

The preceding technologies allow us to pack NWs at a tight pitch into crossbars with programmable cross points at their junctions. The pitch of the NWs can be much smaller than our lithographic patterning. We will be using the crosspoint programmability to configure logic functions into our nanoscale devices. In order to do this, we need a way to selectively place a defined voltage on a single row and column wire in order to set the state of the cross point.
By constructing NWs with doping profiles on their ends, we can give each NW an address. The dimensions of the address bit control regions can be set to the lithographic pitch so that a set of crossed, lithographic wires can be used to address a single NW. If we code up all the NWs along one dimension of an array with suitably different codes, we can get unique NW addressability and effectively implement a demultiplexer between a small number of lithographic wires and a large number of NWs. We cannot control exactly which NW codes appear in a single array or how they are aligned, but if we randomly select NWs from a sufficiently large code space,
we will achieve uniqueness with very high probability (over 99% easily achievable). The addresses do not have to be
entirely unique for this application; allowing a little redundancy will allow us to use a tighter code space.

PROGRAMMABLE WIRED OR:

The arrays can also be served as programmable wired OR planes. Since we have a way to program the cross points into a high or low resistance stage we can make a OR logic into cross point array. We are assuming that each row is in logic low state if it is not driven by a voltage source. When we are driving a column NW to logic high level row NW will be charged up to logic high level. One problem with this structure that Mickey has mentioned was that the output NWs do pull their current directly off the inputs and may not be driven as high as the input voltage. So when you want to drive another array that would be an important problem. But it is overcome with array restoration devices.

DECODERS:
Decoders are needed when lithographic scale wires are connected small diameter NWs. The contacts between nanowires are big meso-scale wires. In order to achieve a high density in a nanowire crossbar each nanowire should not be connected to a distinct meso-scale wire. So we need a decoding algorithm for choosing one nanowire from bunch of nanowires. An adressing scheme is needed for this type of a connection. To program any diode crosspoint in the orplanes we drive one address into the top address decoder and the second into the bottom.

NW CODING: NW coding is a way to build a decoder for connecting NWs to other connections. By using axial doping or material composition profile with Nws, an address for each nanowire can be placed. Since every nanowire has a slightly different address we have to make sure that the doping profile guarantees that. Each region is doped heavily meaning those regions are not affected by field applied by meso-scale wire and each region is doped lightly so that they can be controlled by mesoscale wire. NW will conduct if all of the lithographic-scale wires crossing its lightly doped, controllable regions have a suitable voltage to allow conduction. By selectively making bit regions on each Nws either heavily or lightly doped, we can give the addresses of NWs. Because of heavily doped regions will be conduct such NW in that region with high threshold and also lightly doped regions will be conducted with lower threshold. So, we can control which regions of NW are gate-able. This is also compatible with ongoing

assembly technology if we make the address space for NW large so that we have a high probability that each nanowire has a unique address. In the end of the discussion Mickey pointed the question "Given a set of n NWs, draw ten NWs from it at random with replacement. Determine how large n must be so that with probability .99 at least 5 different NWs appear."
Answer is 12.