

Wire-Streaming Processors (WiSP) on 2-D Nanowire Fabrics

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Motivation

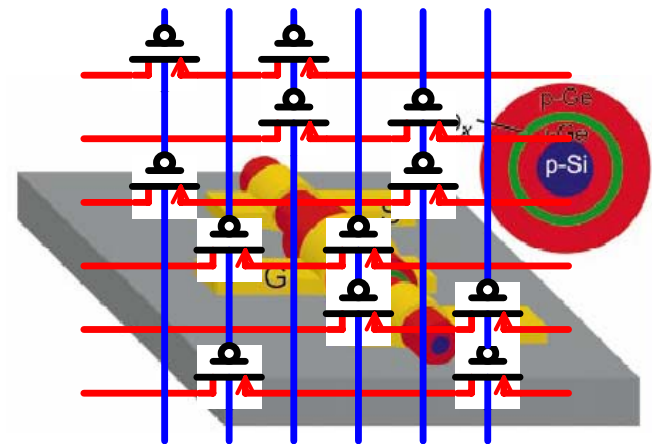
- Most nanotechnology research is focusing on the device level
- It is unclear if there is any advantage with nanoscale systems compared to traditional CMOS systems
 - No work on the design and evaluation of circuits and suitable architectures
 - Significant challenges due to topological, device, and manufacturing constraints
- Density advantages lost with conventional designs if applied to new nanoscale devices

Our focus

- Design of suitable circuits and architectures with nanodevices such as Silicon Nanowires
 - NASIC project: Nanoscale ASICs
 - A complete design of a simple stream processor WiSP based on NASIC circuits and comparison with its CMOS implementation
- Recent publications:
 - "Wire-Streaming Processors on 2-D Nanowire Fabrics", *Nanotech'05, Nano Science and Technology Institute*
 - "Latching on the Wire and Pipelining in Nanoscale Designs", *Non-Silicon Computation Workshop'04*
 - "Opportunities and Challenges in Application-Tuned Circuits and Architectures Based on Nanodevices", *Computer Frontiers'04, ACM SIGMicro*
 - "NASIC: Nanoscale Application-Specific ICs and Architectures", *Boston Area Computer Architecture Workshop'04*

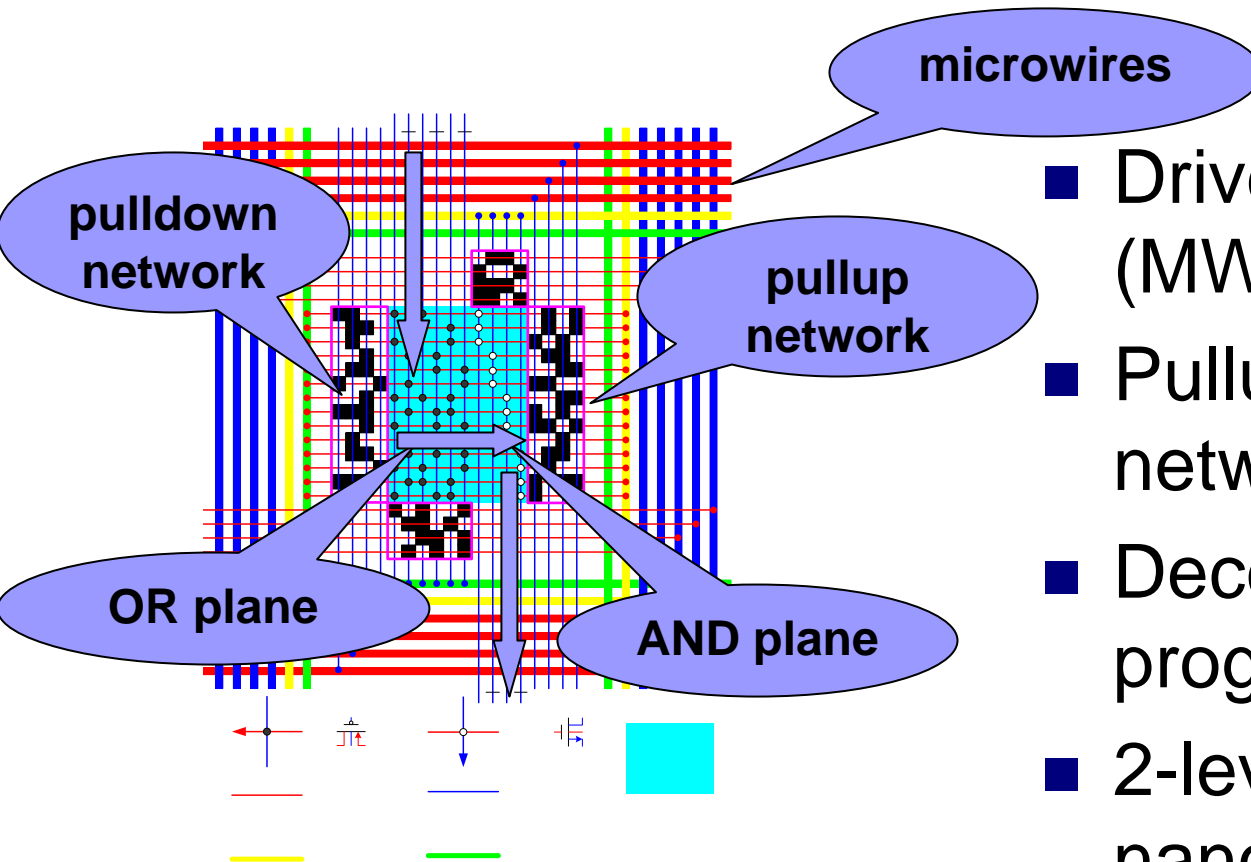
Background - Devices

- Promising technologies in nanodevices:
 - Carbon nanotubes (CNTs) - C.Dekker, et al 1999
 - Silicon nanowires (SiNWs) - A.M.Morales, et al 1998
- Diode and switching elements
 - Diode effect - T.Rueckes, et al 2000
 - FET effect - Y.Huang, et al 2000
- Build Nanogrid with CNTs or SiNWs
 - Nano letter - X. F. Duan, et al 2002



Lauhon et al., Nature 420,57

Background - NASICs



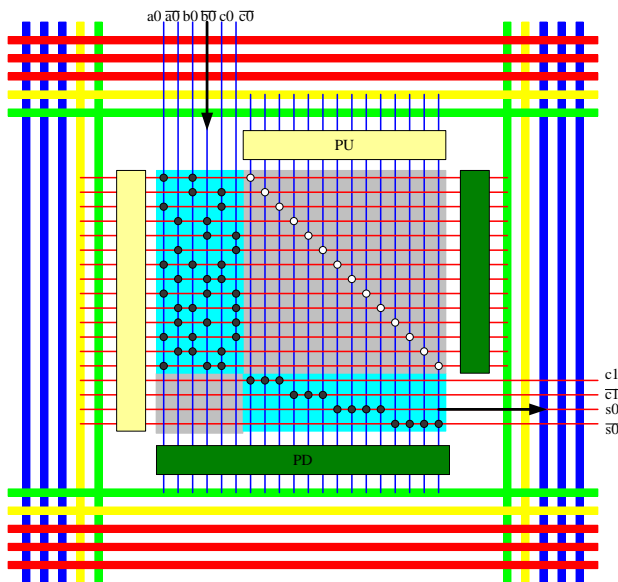
- Driven by microwires (MWs)
- Pullup/pulldown network
- Decoder imprint programming
- 2-level logic in nanoarray

Example of Challenges

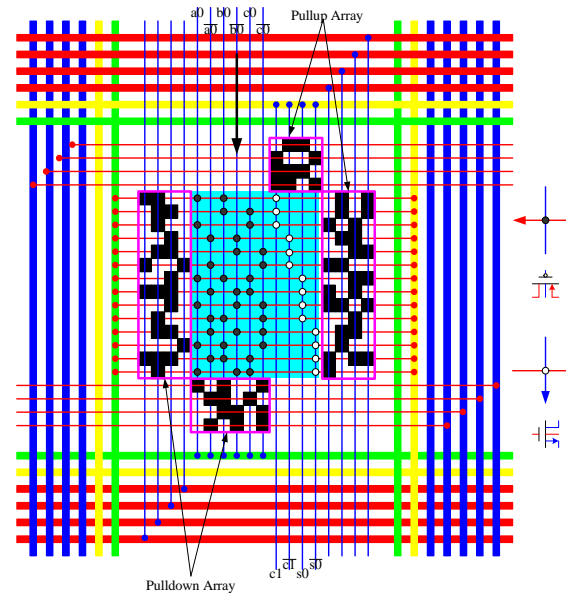
- Circuit and architectural limitations
 - Topology limitations: diagonal problem
 - Sequential circuits, e.g., latches
 - Memories
 - Control paths and forwarding of data
 - Interconnection between tiles
 - Fault tolerance
 - Scalability of 2-level logic
 - Power density

Diagonal Problem

- Turn-the-corner problem
- 2-D fabric often causes only the area on the diagonal can be used

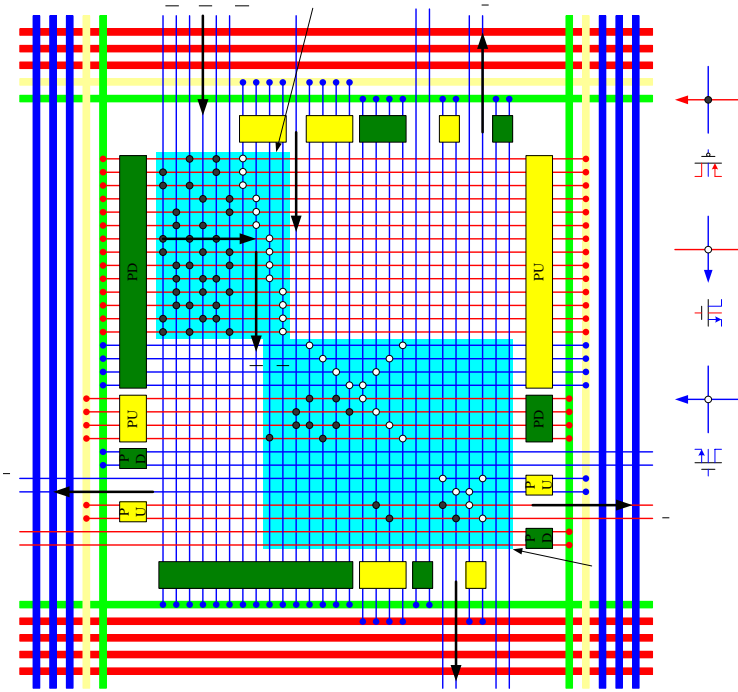


NOR-NOR Logic



OR-AND Logic

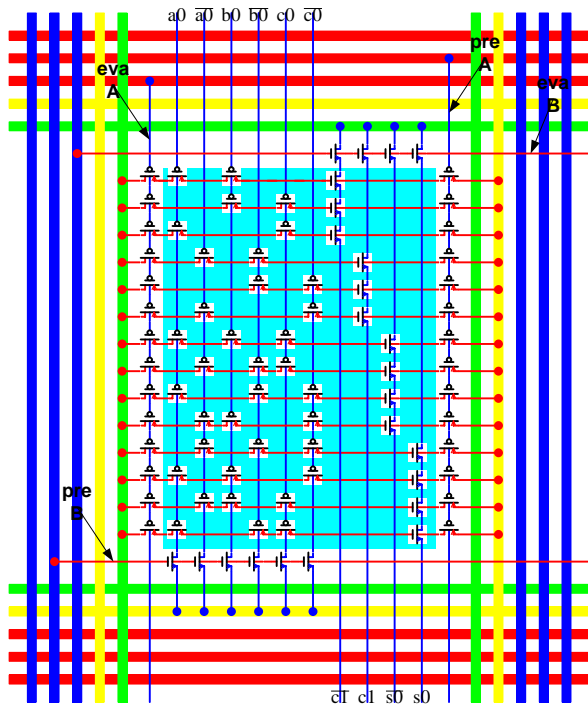
Data Storage on Nanogrids



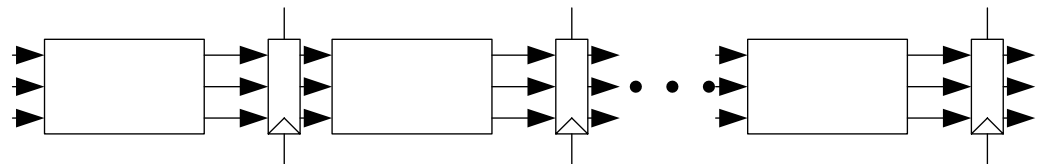
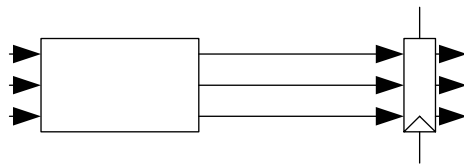
An adder and a Flip-flop

- The circuit has a poor area efficiency
- It requires complicated manufacturing
- It deteriorates area efficiency for diagonal problem

Dynamic Nanotile and Pipeline



- Nano-Latch is implicit latching on the NW
- Precharge and evaluate nanowires
- Nano-Latch provides temporary data storage
- Pipelined structure possible
 - applicability for high-density **stream processing**

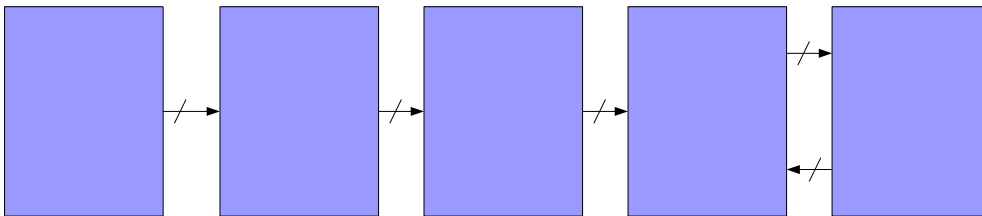


Design Principles

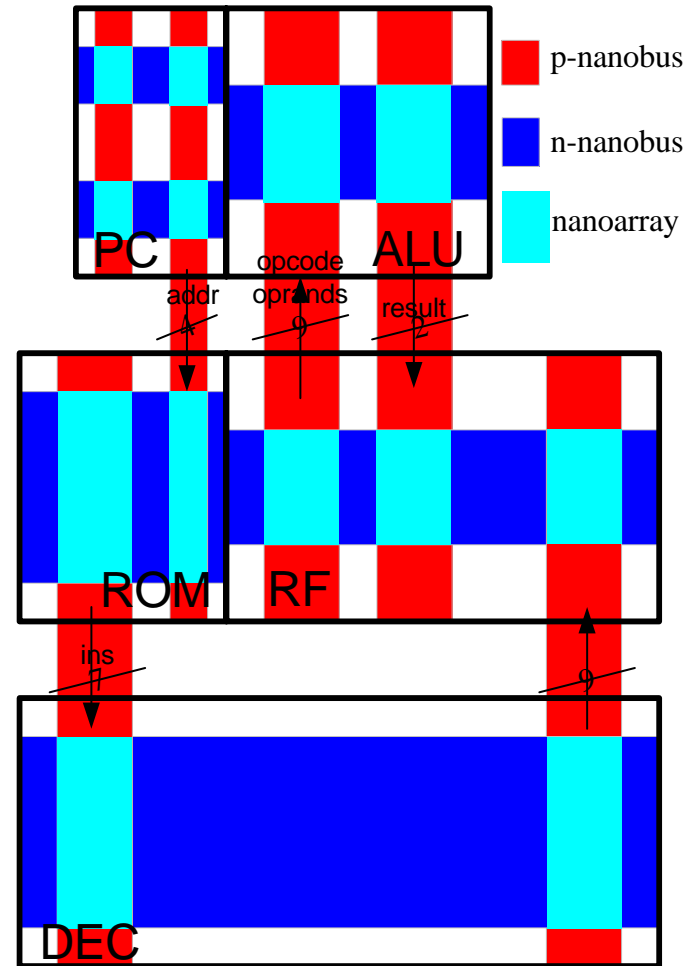
- Make designs tuned to specific application
 - Carefully place nanowires and interconnections between nanowires
 - Optimized NASIC circuits for 2-D fabrics
 - Maximize the usage of nano-latches to improve area efficiency in local storage
 - Pipelining with nanolatches and dynamic NASICs
 - Minimal control and explicit forwarding in the ISA

WiSP-0: Overview

- WiSP-0 is a simple but complete design exercising the principles of NASIC design
- Simple ISA: nop, movi, mov, add, mul
- 5-stage pipeline on 5 NASIC tiles



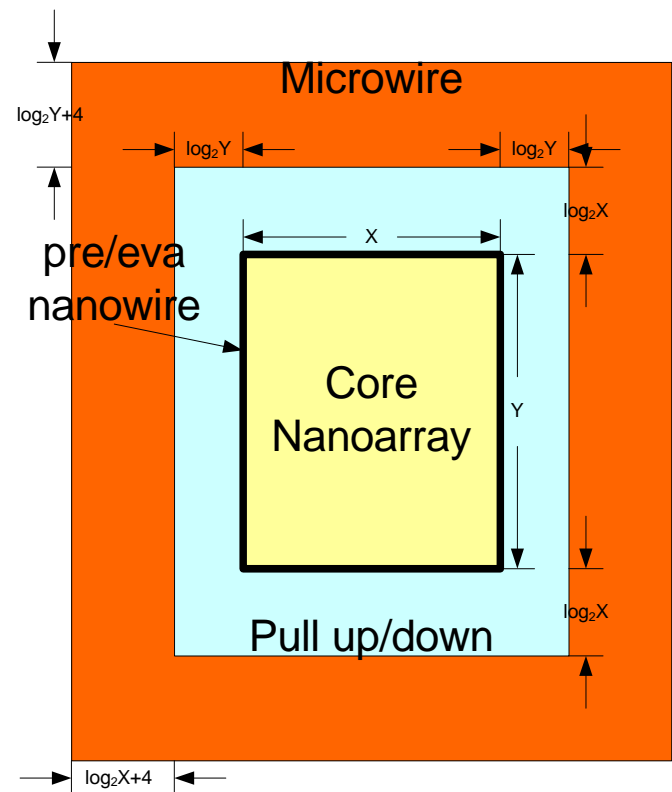
Schematic of WiSP-0



Floorplan of WiSP-0

Comparison with CMOS

- We developed a CMOS prototype in Verilog and synthesized it with Synopsys Design Compiler
- In CMOS
 - Total area is $4,098\mu\text{m}^2$ in 180nm technology and $113\mu\text{m}^2$ when scaled to 30nm technology
- In SiNW
 - Core area is $0.77\mu\text{m}^2$ and total area is $9.04\mu\text{m}^2$
- Density ratio is **12.5**
 - Mainly due to that microwires are significant overhead at this size of a design
- A more suitable core array size is 1,000x1,000 NWs
 - Area efficiency goes up to 76%, then the
 - Density ratio is about **115!**



Conclusions

- Considerable challenges with SiNW based designs
- WiSP-0: simple stream processor based on 2-D fabric
- Huge improvement in density compared to using CMOS approach on SiNWs (i.e., without NASIC optimizations)
- Power density and fault tolerance aspects of WiSP are part of our ongoing work
- NSTI 2005 paper describes WiSP in more depth



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Thank you!