Syllabus
EN292–S10: Advanced Computer Architecture
Semester I 2006–2007
TuTh 1:00pm – 2:20pm, Room 245

Instructor: Iris Bahar, BH 322, phone: 3-1430, email: Iris_Bahar@.Brown.edu

COURSE DESCRIPTION

Computers are designed at three levels. The lowest level involves intricate knowledge of circuits. The middle level involves the logical specification of a hardware system using a hardware definition language like Verilog. The highest, most abstract, level also involves simulation of the computer, but not at the level of individual gates. In this class, we investigate computer architecture with a particular focus on microprocessor design. We will concentrate at the highest level of abstraction.

This class explores current trends and future directions in processor microarchitecture. We will explore various hardware and software techniques designed to maximize parallelism and improve performance keeping in mind technology trends and limitations. Topics include:

- Front-end design (branch prediction, instruction fetch, trace caches)
- HW/SW techniques for exposing more parallelism
- Memory system design (caching, prefetching)
- Technology issues (low power, scaling, reliability, nanotechnology)
- Chip multiprocessors

Class will include a mix of lectures and discussions on assigned readings of recent publications. Students will be responsible for leading and participating in these discussions. A course project exploring a particular topic in depth will be required.

COURSE MATERIAL

Required: *Modern Processor Design: Fundamentals of Superscalar Processors*, by John P. Shen and Mikko Lipasti, McGraw-Hill Publishers, 2004. ISBN: 0-07-057064-7

References:

- *Superscalar Microprocessor Design*, by Mike Johnson, Prentice-Hall, 1991.
- *Computer Architecture: A Quantitative Approach*, 3rd edition, by Hennessy and Patterson, Morgan Kaufmann Publishers, 2003.
- *Readings in Computer Architecture*, edited by M.D. Hill, N.P. Jouppi, and G.S. Sohi, Morgan Kaufmann Publishers, 2000.

In addition, current research papers will be handed out throughout the semester.

LECTURES

To make sure everyone in class is up to speed with the background necessary for this course, approximately the first half of this course will be devoted to course lectures on the basics of superscalar microprocessor design, including instruction fetch and branch prediction, out-of-order execution, memory scheduling, and software scheduling.

DISCUSSION

After the lecture portion of the course, most classes will consist of a discussion of one or two papers on a particular topic in microprocessor architecture. All students are expected to read the papers. There will be one discussion leader and one scribe assigned for each class. The discussion leader is responsible for keeping the discussion going and/or preparing a formal presentation of the material. The scribe will create notes of the lecture which will be posted on the web in a timely fashion. It is expected that *ALL* students be involved in active discussion of the papers.

PROJECT

The project will involve investigating some aspect of high-performance microprocessor architecture via simulation. For example, you may develop and evaluate new branch prediction algorithms, prefetch strategies, or machine organizations. Typically, a project will investigate one of the areas discussed during class; however, you are free to propose any research topic in microprocessor architecture. Group projects are encouraged.

EXAMS

There will be a midterm for this course tentatively scheduled for October 26, 2006, in class. In addition, we will have final project presentations on December 15, 2006, the scheduled day of the final.

GRADING

Following is a breakdown for the course grading.

Class Presentation(s) (leading and scribing): 20%
Midterm Exam: 20%
Homework/Labs: 25%
Class Participation: 10%
Final Project: 25%