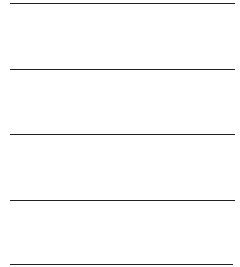


Introduction 1



1.1 OVERVIEW

The ADSP-2106x SHARC—Super Harvard Architecture Computer—is a high-performance 32-bit digital signal processor for speech, sound, graphics, and imaging applications. The SHARC builds on the ADSP-21000 Family DSP core to form a complete system-on-a-chip, adding a dual-ported on-chip SRAM and integrated I/O peripherals supported by a dedicated I/O bus. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Four independent buses for dual data, instructions, and I/O, plus crossbar switch memory connections, comprise the Super Harvard Architecture of the ADSP-2106x.

The ADSP-2106x SHARC represents a new standard of integration for digital signal processors, combining a high-performance floating-point DSP core with integrated, on-chip features including a host processor interface, DMA controller, serial ports, and link port and shared bus connectivity for glueless DSP multiprocessing.

Figure 1.1 illustrates the Super Harvard Architecture of the ADSP-2106x: a crossbar bus switch connecting the core numeric processor to an independent I/O processor, dual-ported memory, and parallel system bus port. Figure 1.2 shows a detailed block diagram of the processor, illustrating the following architectural features:

- 32-Bit IEEE Floating-Point Computation Units—Multiplier, ALU, and Shifter
- Data Register File
- Data Address Generators (DAG1, DAG2)
- Program Sequencer with Instruction Cache
- Interval Timer
- Dual-Ported SRAM
- External Port for Interfacing to Off-Chip Memory & Peripherals
- Host Port & Multiprocessor Interface
- DMA Controller
- Serial Ports
- Link Ports
- JTAG Test Access Port

1 Introduction

Figure 1.2 also shows the three on-chip buses of the ADSP-2106x: the PM bus (program memory), DM bus (data memory), and I/O bus. The PM bus is used to access either instructions or data. During a single cycle the processor can access two data operands, one over the PM bus and one over the DM bus, an instruction (from the cache), and perform a DMA transfer.

The ADSP-2106x's external port provides the processor's interface to external memory, memory-mapped I/O, a host processor, and additional multiprocessing ADSP-2106xs. The external port performs internal and external bus arbitration as well as supplying control signals to shared, global memory and I/O devices.

Figure 1.3 illustrates a typical single-processor system. A multiprocessor system is shown in Chapter 7, *Multiprocessing*.

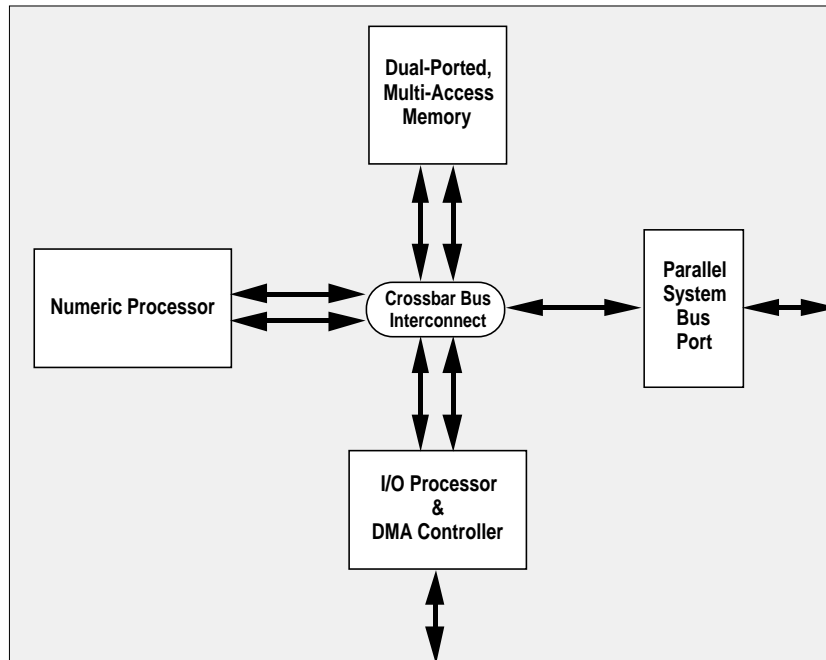


Figure 1.1 Super Harvard Architecture

Introduction 1

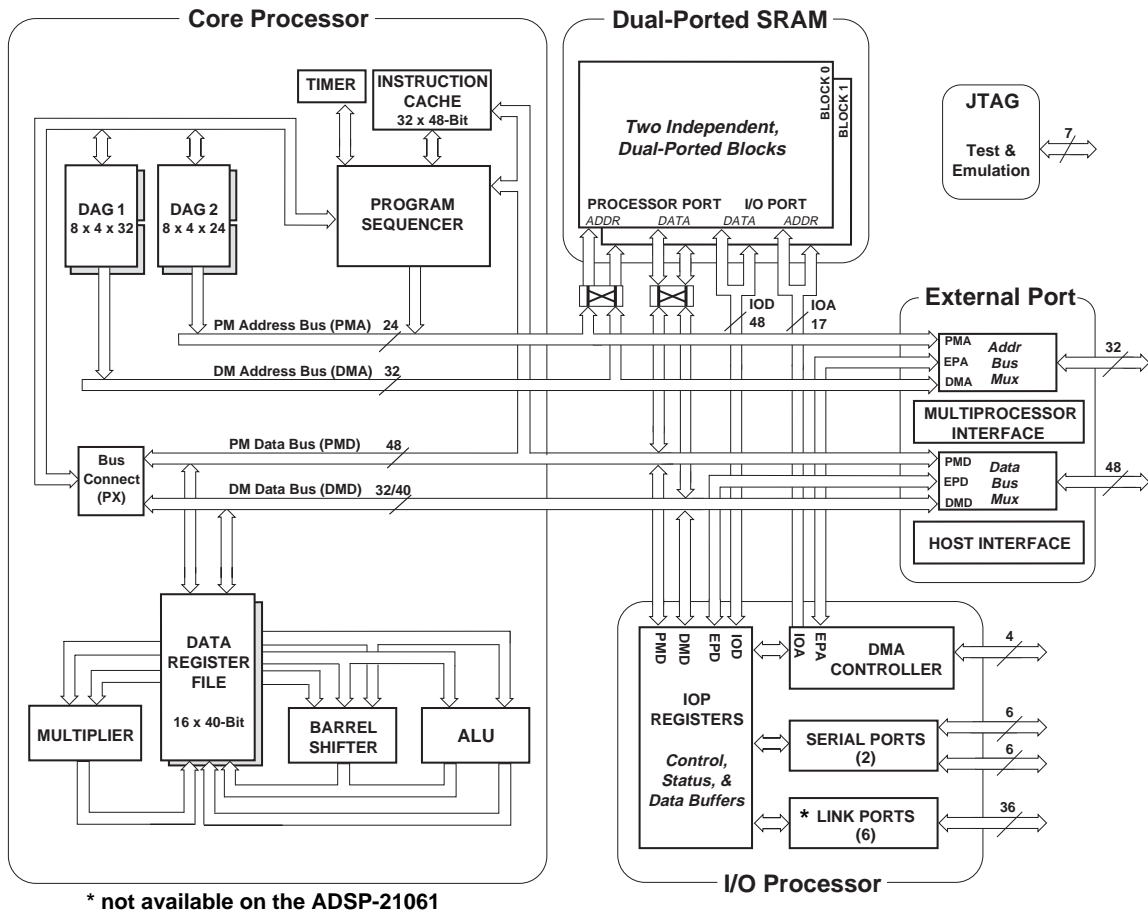


Figure 1.2 ADSP-2106x SHARC Block Diagram

This user's manual contains architectural information and an instruction set description required for the design and programming of ADSP-2106x-based systems. In addition to this manual, hardware designers should refer to the *ADSP-21060/62 Data Sheet* and the *ADSP-21061 Data Sheet* for timing, electrical, and package specifications.

1 Introduction

This manual covers three ADSP-2106x processors: the ADSP-21060, ADSP-21062, and ADSP-21061. The ADSP-21060 contains 4 megabits of on-chip SRAM, the ADSP-21062 contains 2 megabits, and the ADSP-21061 contains 1 megabit. The *Memory* chapter of this manual describes the differences in memory architecture and programming considerations of the three processors. All three processors are code- and function-compatible with the ADSP-21020 processor. With the exception of memory size, the ADSP-21060 and ADSP-21062 are identical in all other aspects as well. Besides memory size, there are four differences between these two processors and the ADSP-21061:

- No link ports on the ADSP-21061
- 6 DMA channels — 4 for serial port and 2 for external port (instead of 4)
- Additional features and changes in DMA for the serial port
- New `idle 16` instruction for a further reduced power mode

These differences are described in detail in the *DMA*, *Serial Port*, and *Program Sequencer* chapters.

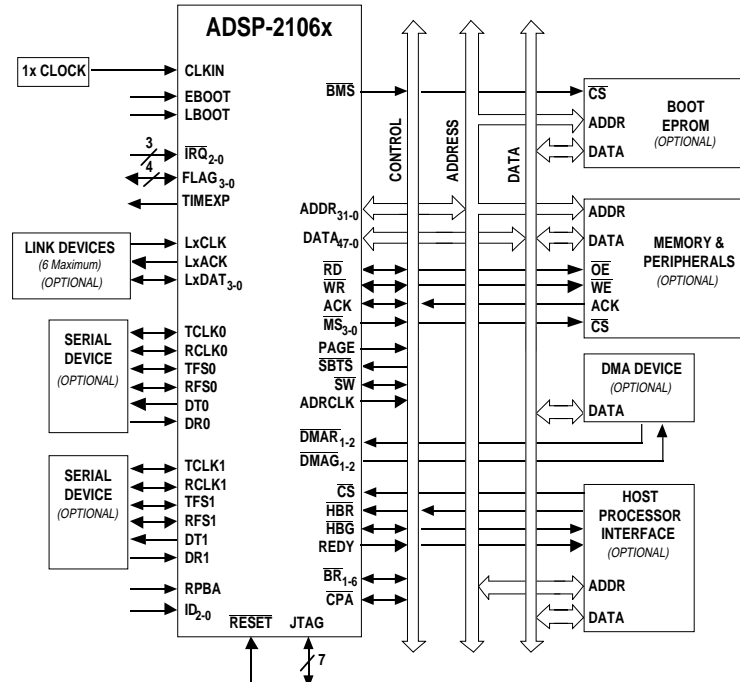


Figure 1.3 ADSP-2106x System

Introduction 1

1.2 ADSP-21000 FAMILY FEATURES & BENEFITS

The ADSP-2106x SHARC processors belong to the ADSP-21000 Family of floating-point digital signal processors (DSPs). The ADSP-21000 Family architecture further addresses the five central requirements for DSPs established in the ADSP-2100 Family of 16-bit fixed-point DSPs:

- Fast, flexible arithmetic computation units
- Unconstrained data flow to and from the computation units
- Extended precision and dynamic range in the computation units
- Dual address generators
- Efficient program sequencing

Fast, Flexible Arithmetic. The ADSP-21000 Family processors execute all instructions in a single cycle. They provide both fast cycle times and a complete set of arithmetic operations including Seed $1/X$, Seed $1/\sqrt{X}$, Min, Max, Clip, Shift, and Rotate, in addition to the traditional multiplication, addition, subtraction, and combined multiplication/addition. The processors are IEEE floating-point compatible and allow either interrupt on arithmetic exception or latched status exception handling.

Unconstrained Data Flow. The ADSP-2106x has an enhanced Harvard architecture combined with a 10-port data register file. In every cycle:

- Two operands can be read or written to or from the register file,
- Two operands can be supplied to the ALU,
- Two operands can be supplied to the multiplier, and
- Two results can be received from the ALU and multiplier.

The processor's 48-bit orthogonal instruction word supports fully parallel data transfer and arithmetic operations in the same instruction.

40-Bit Extended Precision. The ADSP-21000 Family processors handle 32-bit IEEE floating-point format, 32-bit integer and fractional formats (twos-complement and unsigned), and extended-precision 40-bit IEEE floating-point format. The processors carry extended precision throughout their computation units, limiting intermediate data truncation errors. When working with data on-chip, the extended-precision 32-bit mantissa can be transferred to and from all computation units. The 40-bit data bus may be extended off-chip if desired. The fixed-point formats have an 80-bit accumulator for true 32-bit fixed-point computations.

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Dual Address Generators. The ADSP-21000 Family processors have two data address generators (DAGs) that provide immediate or indirect (pre- and post-modify) addressing. Modulus and bit-reverse operations are supported with no constraints on data buffer placement.

Efficient Program Sequencing. In addition to zero-overhead loops, the ADSP-21000 Family processors support single-cycle setup and exit for loops. Loops are both nestable (six levels in hardware) and interruptable. The processors support both delayed and non-delayed branches.

1.2.1 System-Level Enhancements

The ADSP-21000 Family processors include several enhancements that simplify system development. The enhancements occur in three key areas:

- Architectural features supporting high-level languages and operating systems
- IEEE 1149.1 JTAG serial scan path and on-chip emulation features
- Support of IEEE floating-point formats

High Level Languages. The ADSP-21000 Family architecture has several features that directly support high-level language compilers and operating systems:

- General purpose data and address register files
- 32-bit native data types
- Large address space
- Pre- and post-modify addressing
- Unconstrained circular data buffer placement
- On-chip program, loop, and interrupt stacks

Additionally, the ADSP-21000 Family architecture is designed specifically to support ANSI-standard Numerical C extensions—the first compiled language to support vector data types and operators for numeric and signal processing.

Serial Scan and Emulation Features. The ADSP-21000 Family processors support the IEEE standard P1149.1 Joint Test Action Group (JTAG) standard for system test. This standard defines a method for serially scanning the I/O status of each component in a system. The JTAG serial port is also used by the ADSP-2106x EZ-ICE to gain access to the processor's on-chip emulation features.

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IEEE Formats. The ADSP-21000 Family processors support IEEE floating-point data formats. This means that algorithms developed on IEEE-compatible processors and workstations are portable across processors without concern for possible instability introduced by biased rounding or inconsistent error handling.

1.2.2 Why Floating-Point DSP?

A digital signal processor's data format determines its ability to handle signals of differing precision, dynamic range, and signal-to-noise ratios. However, ease-of-use and time-to-market considerations are often equally important.

Precision. The number of bits of precision of A/D converters has continued to increase, and the trend is for both precision and sampling rates to increase.

Dynamic Range. Compression and decompression algorithms have traditionally operated on signals of known bandwidth. These algorithms were developed to behave regularly, to keep costs down and implementations easy. Increasingly, however, the trend in algorithm development is not to constrain the regularity and dynamic range of intermediate results. Adaptive filtering and imaging are two applications requiring wide dynamic range.

Signal-to-Noise Ratio. Radar, sonar and even commercial applications like speech recognition require wide dynamic range in order to discern selected signals from noisy environments.

Ease-of-Use. In general, 32-bit floating-point DSPs are easier to use and allow a quicker time-to-market than 16-bit fixed-point processors. The extent to which this is true depends on the floating-point processor's architecture. Consistency with IEEE workstation simulations and the elimination of scaling are two clear ease-of-use advantages. High-level language programmability, large address spaces, and wide dynamic range allow system development time to be spent on algorithms and signal processing concerns rather than assembly language coding, code paging, and error handling.

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1.3 ADSP-2106X ARCHITECTURE

The following sections summarize the features of the ADSP-2106x SHARC architecture. These features are described in greater detail in succeeding chapters.

1.3.1 Core Processor

The core processor of the ADSP-2106x consists of three computation units, a program sequencer, two data address generators, timer, instruction cache, and data register file.

1.3.1.1 Computation Units

The ADSP-2106x core processor contains three independent computation units: an ALU, a multiplier with a fixed-point accumulator, and a shifter. For meeting a wide variety of processing needs, the computation units process data in three formats: 32-bit fixed-point, 32-bit floating-point and 40-bit floating-point. The floating-point operations are single-precision IEEE-compatible. The 32-bit floating-point format is the standard IEEE format, whereas the 40-bit IEEE extended-precision format has eight additional LSBs of mantissa for greater accuracy.

The ALU performs a standard set of arithmetic and logic operations in both fixed-point and floating-point formats. The multiplier performs floating-point and fixed-point multiplication as well as fixed-point multiply/add and multiply/subtract operations. The shifter performs logical and arithmetic shifts, bit manipulation, field deposit and extraction and exponent derivation operations on 32-bit operands.

The computation units perform single-cycle operations; there is no computation pipeline. The units are connected in parallel rather than serially. The output of any unit may be the input of any unit on the next cycle. In a *multifunction* computation, the ALU and multiplier perform independent, simultaneous operations.

1.3.1.2 Data Register File

A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. The register file has two sets (primary and alternate) of sixteen registers each, for fast context switching. All of the registers are 40 bits wide. The register file, combined with the core processor's Harvard architecture, allows unconstrained data flow between computation units and internal memory.

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1.3.1.3 Program Sequencer & Data Address Generators

Two dedicated address generators and a program sequencer supply addresses for memory accesses. Together the sequencer and data address generators allow computational operations to execute with maximum efficiency since the computation units can be devoted exclusively to processing data. With its instruction cache, the ADSP-2106x can simultaneously fetch an instruction (from the cache) and access two data operands (from memory). The data address generators implement circular data buffers in hardware.

The program sequencer supplies instruction addresses to program memory. It controls loop iterations and evaluates conditional instructions. With an internal loop counter and loop stack, the ADSP-2106x executes looped code with zero overhead. No explicit jump instructions are required to loop or to decrement and test the counter.

The ADSP-2106x achieves its fast execution rate by means of pipelined *fetch*, *decode* and *execute* cycles. If external memories are used, they are allowed more time to complete an access than if there were no decode cycle.

The data address generators (DAGs) provide memory addresses when data is transferred between memory and registers. Dual data address generators enable the processor to output simultaneous addresses for two operand reads or writes. DAG1 supplies 32-bit addresses to data memory. DAG2 supplies 24-bit addresses to program memory for program memory data accesses.

Each DAG keeps track of up to eight address pointers, eight modifiers and eight length values. A pointer used for indirect addressing can be modified by a value in a specified register, either before (pre-modify) or after (post-modify) the access. A length value may be associated with each pointer to perform automatic modulo addressing for circular data buffers; the circular buffers can be located at arbitrary boundaries in memory. Each DAG register has an alternate register that can be activated for fast context switching.

Circular buffers allow efficient implementation of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation.

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1.3.1.4 Instruction Cache

The program sequencer includes a 32-word instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only instructions whose fetches conflict with program memory data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

1.3.1.5 Interrupts

The ADSP-2106x has four external hardware interrupts: three general-purpose interrupts, IRQ_{2-0} , and a special interrupt for reset. The processor also has internally generated interrupts for the timer, DMA controller operations, circular buffer overflow, stack overflows, arithmetic exceptions, multiprocessor vector interrupts, and user-defined software interrupts.

For the general-purpose external interrupts and the internal timer interrupt, the ADSP-2106x automatically stacks the arithmetic status and mode (MODE1) registers in parallel with the interrupt servicing, allowing four nesting levels of very fast service for these interrupts.

1.3.1.6 Timer

The programmable interval timer provides periodic interrupt generation. When enabled, the timer decrements a 32-bit count register every cycle. When this count register reaches zero, the ADSP-2106x generates an interrupt and asserts its TIMEXP output. The count register is automatically reloaded from a 32-bit period register and the count resumes immediately.

1.3.1.7 Core Processor Buses

The processor core has four buses: Program Memory Address, Data Memory Address, Program Memory Data, and Data Memory Data. On the ADSP-2106x processors, data memory stores data operands while program memory is used to store both instructions and data (filter coefficients, for example)—this allows dual data fetches, when the instruction is supplied by the cache.

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The PM Address bus and DM Address bus are used to transfer the addresses for instructions and data. The PM Data bus and DM Data bus are used to transfer the data or instructions stored in each type of memory. The PM Address bus is 24 bits wide allowing access of up to 16M words of mixed instructions and data. The PM Data bus is 48 bits wide to accommodate the 48-bit instruction width. Fixed-point and single-precision floating-point data is aligned to the upper 32 bits of the PM Data bus.

The DM Address bus is 32 bits wide allowing direct access of up to 4G words of data. The DM Data bus is 40 bits wide. Fixed-point and single-precision floating-point data is aligned to the upper 32 bits of the DM Data bus. The DM Data bus provides a path for the contents of any register in the processor to be transferred to any other register or to any data memory location in a single cycle. The data memory address comes from one of two sources: an absolute value specified in the instruction code (*direct addressing*) or the output of a data address generator (*indirect addressing*).

1.3.1.8 Internal Data Transfers

Nearly every register in the core processor of the ADSP-2106x is classified as a *universal register*. Instructions are provided for transferring data between any two universal registers or between a universal register and memory. This includes control registers and status registers, as well as the data registers in the register file.

The PX bus connect registers permit data to be passed between the 48-bit PM Data bus and the 40-bit DM Data bus or between the 40-bit register file and the PM Data bus. These registers contain hardware to handle the 8-bit width difference.

1.3.1.9 Context Switching

Many of the processor's registers have alternate registers that can be activated during interrupt servicing to facilitate a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result register all have alternates. Registers active at reset are called *primary* registers, while the others are called *alternate* (or *secondary*) registers. Control bits in a mode control register determine which set of registers is active at any particular time.

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1.3.1.10 Instruction Set

The ADSP-21000 Family instruction set provides a wide variety of programming capabilities. *Multifunction* instructions enable computations in parallel with data transfers, as well as simultaneous multiplier and ALU operations. The addressing power of the ADSP-2106x gives you flexibility in moving data both internally and externally. Every instruction can be executed in a single processor cycle. The ADSP-21000 Family assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

1.3.2 Dual-Ported Internal Memory

The ADSP-21060 contains 4 megabits of on-chip SRAM, organized as two blocks of 2 Mbits each, which can be configured for different combinations of code and data storage. The ADSP-21062 includes a 2 Mbit SRAM, organized as two 1 Mbit blocks. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle.

All of the memory can be accessed as 16-bit, 32-bit, or 48-bit words. On the ADSP-21060, the memory can be configured as a maximum of 128K words of 32-bit data, 256K words of 16-bit data, 80K words of 48-bit instructions (and 40-bit data), or combinations of different word sizes up to 4 megabits. On the ADSP-21062, the memory can be configured as a maximum of 64K words of 32-bit data, 128K words of 16-bit data, 40K words of 48-bit instructions (and 40-bit data), or combinations of different word sizes up to 2 megabits. On the ADSP-21061, the memory can be configured as a maximum of 32K words of 32-bit data, 64K words of 16-bit data, 16K words of 48-bit instructions (and 40-bit data), or combinations of different word sizes up to 1 megabit.

A 16-bit floating-point storage format is supported which effectively doubles the amount of data that may be stored on chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction.

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While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-2106x's external port.

1.3.3 External Memory & Peripherals Interface

The ADSP-2106x's external port provides the processor's interface to off-chip memory and peripherals. The 4-gigaword off-chip address space is included in the ADSP-2106x's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 48-bit data bus. External SRAM can be either 16, 32, or 48 bits wide; the ADSP-2106x's on-chip DMA controller automatically packs external data into the appropriate word width, either 48-bit instructions or 32-bit data.

Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-2106x provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold, and disable time requirements.

1.3.4 Host Processor Interface

The ADSP-2106x's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds up to the full clock rate of the ADSP-2106x are supported. The host interface is accessed through the ADSP-2106x's external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead. The host can directly read and write the internal memory of the ADSP-2106x, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

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1.3.5 Multiprocessing

The ADSP-2106x offers powerful features tailored to multiprocessing DSP systems. The unified address space allows direct interprocessor accesses of each ADSP-2106x's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-2106xs and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Processor bus lock allows indivisible *read-modify-write* sequences for semaphores. A vector interrupt capability is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 240 Mbytes/sec over the link ports or external port. *Broadcast writes* allow simultaneous transmission of data to all ADSP-2106xs and can be used to implement reflective semaphores.

1.3.6 I/O Processor

The ADSP-2106x's I/O Processor (IOP) includes two serial ports, six 4-bit link ports, and a DMA controller.

1.3.6.1 Serial Ports

The ADSP-2106x features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at the full clock rate of the processor, providing each with a maximum data rate of 40 Mbit/s. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports offers a TDM multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 to 32 bits. They offer selectable synchronization and transmit modes as well as optional μ -law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated.

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1.3.6.2 Link Ports

The ADSP-21062 and ADSP-21060 feature six 4-bit link ports that provide additional I/O capabilities. The link ports can be clocked twice per cycle, allowing each to transfer 8 bits per cycle. Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems.

The link ports can operate independently and simultaneously, with a maximum data throughput of 240 Mbytes/s. Link port data is packed into 32-bit or 48-bit words, and can be directly read by the core processor or DMA-transferred to on-chip memory. Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

There are no link ports on the ADSP-21061.

1.3.6.3 DMA Controller

The ADSP-2106x's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program. Both code and data can be downloaded to the ADSP-2106x using DMA transfers.

DMA transfers can occur between the ADSP-2106x's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-2106x's internal memory and its serial ports or link ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16, 32, or 48-bit words is automatically performed during DMA transfers.

Ten channels of DMA are available on the ADSP-21060 and ADSP-21062—two via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other ADSP-2106xs, memory or I/O transfers). Four additional link port DMA channels are shared with serial port 1 and the external port. There are six channels of DMA available on the ADSP-21061—four via the serial ports and two via the external port. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($DMAR_{1-2}$, $DMAG_{1-2}$). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

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The ten DMA channels of the ADSP-21060 and ADSP-21062 are numbered as shown below:

<u>DMA Channel#</u>	<u>Data Buffer</u>	<u>Description</u>
DMA Channel 0	RX0	Serial Port 0 Receive
DMA Channel 1	RX1 (or LBUF0)	Serial Port 1 Receive (or Link Buffer 0)
DMA Channel 2	TX0	Serial Port 0 Transmit
DMA Channel 3	TX1 (or LBUF1)	Serial Port 1 Transmit (or Link Buffer 1)
DMA Channel 4	LBUF2	Link Buffer 2
DMA Channel 5	LBUF3	Link Buffer 3
DMA Channel 6	EPB0 (or LBUF4)	Ext. Port FIFO Buffer 0 (or Link Buffer 4)
DMA Channel 7 *	EPB1 (or LBUF5)	Ext. Port FIFO Buffer 1 (or Link Buffer 5)
DMA Channel 8 *	EPB2	Ext. Port FIFO Buffer 2
DMA Channel 9	EPB3	Ext. Port FIFO Buffer 3

* $\overline{DMAR1}$ and $\overline{DMAG1}$ are handshake controls for DMA Channel 7.
 $\overline{DMAR2}$ and $\overline{DMAG2}$ are handshake controls for DMA Channel 8.

1.3.6.4 Booting

The internal memory of the ADSP-2106x can be booted at system powerup from an 8-bit EPROM or a host processor. Additionally, the ADSP-21060 and the ADSP-21062 can also be booted through one of the link ports. Selection of the boot source is controlled by the BMS, EBOOT, and LBOOT pins. Both 32-bit and 16-bit host processors can be used for booting.

1.4 DEVELOPMENT TOOLS

The ADSP-2106x is supported with a complete set of software and hardware development tools, including an EZ-LAB[®] Evaluation Board, EZ-ICE[®] In-Circuit Emulator, and development software. The development software provides tools for programming and debugging applications in both assembly language and C. The EZ-ICE emulator allows system integration and hardware/software debugging. Figure 1.4 shows the process of developing an application using the development tools.

The development software includes an ANSI C Compiler. The compiler includes Numerical C extensions based on the work of the ANSI NCEG committee (Numerical C Extensions Group).

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Numerical C provides extensions to the C language for array selection, vector math operations, complex data types, circular pointers, and variably-dimensioned arrays. Other components of the development software include a C Runtime Library with custom DSP functions, C and assembly language Debugger, Assembler, Assembly Library/Librarian, Linker, and Simulator.

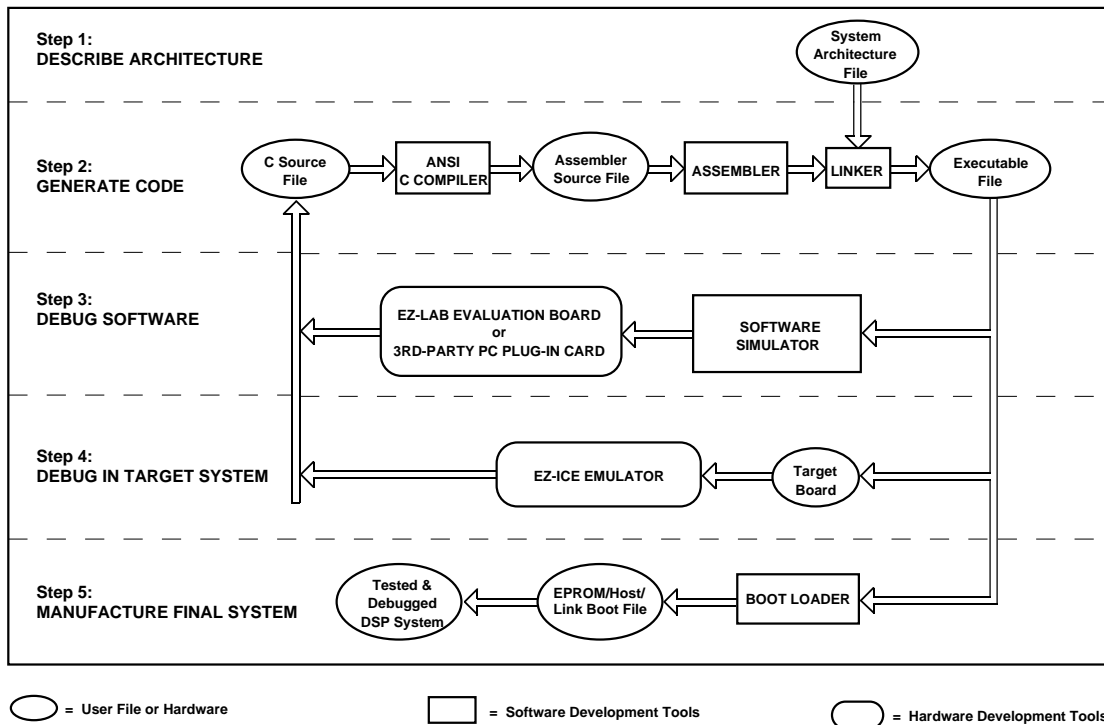


Figure 1.4 System Design and Development Process

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The ADSP-2106x EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x processor to monitor and control the target board processor during emulation. The EZ-ICE provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Non-intrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

Further details and ordering information are available in the *ADSP-21000 Family Hardware & Software Development Tools* data sheet. This data sheet can be requested from any Analog Devices sales office or distributor.

1.5 MESH MULTIPROCESSING

Mesh multiprocessing is a parallel processing system architecture that offers high throughput, system flexibility, and software simplicity. The ADSP-21060 and ADSP-21062 SHARC processors include features which specifically support this system architecture. Mesh multiprocessing systems are suited to a wide variety of applications including wide-area airborne radar systems, interactive medical imaging, virtual reality, high-speed engineering simulations, neural networks, and solutions of large systems of linear equations.

1.6 ADDITIONAL LITERATURE

The following publications can be ordered from any Analog Devices sales office.

ADSP-21060/62 SHARC Data Sheet

ADSP-21061 SHARC Data Sheet

ADSP-21000 Family Hardware & Software Development Tools Data Sheet

ADSP-21000 Family Assembler Tools & Simulator Manual

ADSP-21000 Family C Tools Manual

ADSP-21000 Family C Runtime Library Manual

ADSP-21000 Family Applications Handbook, Vol. 1