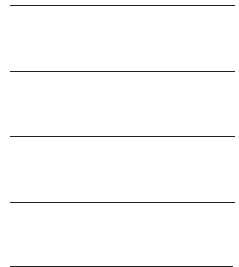


# SHARC Glossary G



<u>Term</u>	<u>Definition</u>
core processor <i>or</i> processor core	ADSP-21000 core DSP processor—program sequencer, instruction cache, timer, DAG1, DAG2, register file (R15-0), computation units. Does not include ADSP-2106x's internal memory, external port, and I/O processor.  An “action performed by the core processor” implies an action caused by the program executing on the ADSP-2106x. This is in contrast to an action performed by the on-chip DMA controller or by an external bus master, either host processor or another ADSP-2106x.
external bus	DATA <sub>47-0</sub> , ADDR <sub>31-0</sub> , $\overline{RD}$ , $\overline{WR}$ , $\overline{MS}_{3-0}$ , $\overline{BMS}$ , ADRCLK, PAGE, $\overline{SW}$ , ACK, and SBTS signals
multiprocessor system	a system with multiple ADSP-2106xs, with or without a host processor; the ADSP-2106xs are connected by the external bus and/or link ports
multiprocessor memory space	portion of the ADSP-2106x's memory map that includes the internal memory and IOP registers of each ADSP-2106x in a multiprocessing system; this address space is mapped into the unified address space of the ADSP-2106x
IOP register	one of the control, status, or data buffer registers of the ADSP-2106x's on-chip I/O processor
bus slave <i>or</i> slave mode	an ADSP-2106x can be a bus slave to another ADSP-2106x or to a host processor (the ADSP-2106x becomes a host slave when the HBG signal is returned)

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bus transition cycle (BTC)	a cycle in which control of the external bus is passed from one ADSP-2106x to another (in a multiprocessor system)
host transition cycle (HTC)	a cycle in which control of the external bus is passed from the ADSP-2106x to the host processor—during this cycle the ADSP-2106x stops driving the $\overline{RD}$ , $\overline{WR}$ , $ADDR_{31-0}$ , $\overline{MS}_{3-0}$ , $ADRCLK$ , $PAGE$ , $\overline{SW}$ , and $\overline{DMAGx}$ signals, which must then be driven by the host
asynchronous transfers	asynchronous host accesses of the ADSP-2106x; after acquiring control of the ADSP-2106x's external bus, the host must assert the $\overline{CS}$ pin of the ADSP-2106x it wants to access; the ADSP-2106x uses the $REDY$ output to add wait states to an asynchronous access
synchronous transfers	synchronous host accesses of the ADSP-2106x; $\overline{CS}$ is not asserted and the host must act like another ADSP-2106x in a multiprocessor system, by generating an address in multiprocessor memory space, asserting $\overline{WR}$ or $\overline{RD}$ , and driving out or latching in the data; the ADSP-2106x uses $ACK$ to add wait states to a synchronous access
direct reads & writes	a direct access of the ADSP-2106x's internal memory or IOP registers by another ADSP-2106x or by a host processor
external port FIFO buffers	$EPB0$ , $EPB1$ , $EPB2$ , and $EPB3$ —the IOP registers used for external port DMA transfers and single-word data transfers (from other ADSP-2106xs or from a host processor); these buffers are 6-deep FIFOs
single-word data transfers	reads and writes to the $EPBx$ external port buffers, performed externally by the ADSP-2106x bus master or internally by the ADSP-2106x slave's core; these occur when DMA is disabled in the $DMACx$ control register

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single-word data transfers	<i>(host processor)</i> reads and writes to the EPBx external port buffers, performed externally by the host or internally by the ADSP-2106x core; these occur when DMA is disabled in the DMACx control register
link port vs. link buffer	the link ports receive and transmit data on their LxDAT <sub>3-0</sub> data pins; the six independent link buffers may be connected to any of the six link ports
48-bit word	usually implies instruction word, but may also imply 48-bit instructions <i>and</i> 40-bit extended-precision data values that are transferred within 48-bit words; 48-bit words use three 16-bit memory columns
32-bit word	standard 32-bit data word; uses two 16-bit memory columns
16-bit word	16-bit short data word; uses one 16-bit memory column
data memory	region of memory in which 32-bit data words and 16-bit short words are stored; <i>implies that the DM bus is used for accesses</i> (see the following sections in the <i>Memory</i> chapter of this manual for details: “Overview,” “Dual Data Accesses,” and “On-Chip Memory Buses & Address Generation”)
program memory	region of memory in which 48-bit instruction words and (optionally) 32-bit or 40-bit data words are stored; <i>implies that the PM bus is used for accesses</i> (see the following sections in the <i>Memory</i> chapter of this manual for details: “Overview,” “Dual Data Accesses,” “Instruction Cache & PM Bus Data Accesses,” and “On-Chip Memory Buses & Address Generation”)
program memory data access	when an ADSP-2106x instruction reads or writes data over the PM Data Bus; the address is generated by DAG2 on the PM Address Bus
DMACx control registers	the DMA control registers for the EPBx external port buffers: DMAC6, DMAC7, DMAC8, and DMAC9 (corresponding respectively to EPB0, EPB1, EPB2, and EPB3)
DMA control registers	<i>see “DMACx control registers”</i>

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DMA parameter registers	the address (II), modifier (IM), count (C), chain pointer (CP), etc., registers used to set up a DMA transfer
transfer control block (TCB)	a set of DMA parameter register values stored in memory that are downloaded by the ADSP-2106x's DMA controller for chained DMA operations
TCB chain loading	the process in which the ADSP-2106x's DMA controller downloads a TCB from memory and autoinitializes the DMA parameter registers
cycle <i>or</i> processor cycle	one cycle of the ADSP-2106x's CLKIN input
extra cycle	a cycle generated by the ADSP-2106x when an instruction cannot be completed in a single CLKIN cycle (e.g. to allow an additional access of internal or external memory); see "Execution Stalls" in the <i>System Design</i> chapter of this manual
sticky status bit	(in STKY status register) a "sticky" status bit, once set, remains set until it is explicitly cleared (with the status bit manipulation instruction)

## Equivalent Terms

multiprocessor system = multiprocessing system = multiprocessor cluster  
core processor = processor core = ADSP-2106x core  
DMA operation = DMA sequence  
cycle = clock cycle = processor cycle = CLKIN cycle

<u>Acronym</u>	<u>Definition</u>
IOP	I/O Processor
DAG	Data Address Generator
SPORT	Serial Port
PMA	Program Memory Address
DMA	Data Memory Address
PMD	Program Memory Data
DMD	Data Memory Data
EPA	External Port Address
EPD	External Port Data
IOA	I/O Address
IOD	I/O Data