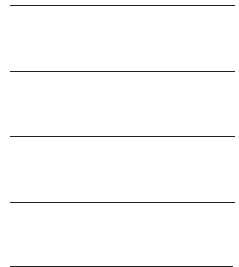


JTAG Test Access Port D



D.1 OVERVIEW

A boundary scan allows a system designer to test interconnections on a printed circuit board with minimal test-specific hardware. The scan is made possible by the ability to control and monitor each input and output pin on each chip through a set of serially scannable latches. Each input and output is connected to a latch, and the latches are connected as a long shift register so that data can be read from or written to them through a serial test access port (TAP). The ADSP-2106x contains a test access port compatible with the industry-standard IEEE 1149.1 (JTAG) specification.

Only the IEEE 1149.1 features specific to the ADSP-2106x are described here. For more information, see the IEEE 1149.1 specification and the references listed at the end of this appendix.

The boundary scan allows a variety of functions to be performed on each input and output signal of the ADSP-2106x. Each input has a latch that monitors the value of the incoming signal and can also drive data into the chip in place of the incoming value. Similarly, each output has a latch that monitors the outgoing signal and can also drive the output in place of the outgoing value. For bidirectional pins, the combination of input and output functions is available.

Every latch associated with a pin is part of a single serial shift register path. Each latch is a master/slave type latch with the controlling clock provided externally. This clock (TCK) is asynchronous to the ADSP-2106x system clock (CLKIN).

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D.2 TEST ACCESS PORT

The test access port (TAP) of the ADSP-2106x controls the operation of the boundary scan. The TAP consists of five pins that control a state machine, including the boundary scan. The state machine and pins conform to the IEEE 1149.1 specification.

TCK (input)	Test Clock. Used to clock serial data into scan latches and control sequencing of the test state machine. TCK can be asynchronous with CLKIN.
TMS (input)	Test Mode Select. Primary control signal for the state machine. Synchronous with TCK. A sequence of values on TMS adjusts the current state of the TAP.
TDI (input)	Test Data Input. Serial input data to the scan latches. Synchronous with TCK.
TDO (output)	Test Data Output. Serial output data from the scan latches. Synchronous with TCK.
$\overline{\text{TRST}}$ (input)	Test Reset. Resets the test state machine. Can be asynchronous with TCK.

A BSDL file for the ADSP-2106x is available on Analog Devices' BBS and Internet ftp site. The BBS can be reached at:

(617) 461-4258 8 data bits, no parity, 1 stop bit,
300/1200/2400/9600/14400 baud

To connect to the ftp site, login as anonymous using your email address for your password and type (from the Unix prompt):

ftp ftp.analog.com (or ftp 137.71.23.11)

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D.3 INSTRUCTION REGISTER

The instruction register allows an instruction to be shifted into the processor. This instruction selects the test to be performed and/or the test data register to be accessed. The instruction register is 5 bits long with no parity bit. A value of 10000 binary is loaded (LSB nearest TDI) into the instruction register whenever the TAP reset state is entered.

Table D.1 lists the binary code for each instruction. Bit 0 is nearest TDI and bit 4 is nearest TDO. An “x” specifies a “don’t-care” state. No data registers are placed into test modes by any of the public instructions. The instructions affect the ADSP-2106x as defined in the 1149.1 specification. The optional instructions RUNBIST, IDCODE and USERCODE are not supported by the ADSP-2106x.

Instruction Bits 4 3 2 1 0	Instruction Name	Register (Serial Path)	Type
1 x x x x	BYPASS	Bypass	Public
0 0 0 0 0	EXTTEST	Boundary	Public
0 0 0 0 1	SAMPLE/PRELOAD	Boundary	Public
0 0 0 1 0	<i>reserved for emulation</i>	—	<i>Private</i>
0 0 0 1 1	INTEST	Boundary	Public
0 0 1 0 0	<i>reserved for emulation</i>	—	<i>Private</i>
0 0 1 0 1	<i>reserved for emulation</i>	—	<i>Private</i>
0 0 1 1 0	<i>reserved for emulation</i>	—	<i>Private</i>
0 0 1 1 1	<i>reserved for emulation</i>	—	<i>Private</i>
0 1 x x x	<i>reserved for emulation</i>	—	<i>Private</i>

Table D.1 Test Instructions

The entry under “Register” is the serial scan path, either Boundary or Bypass in this case, enabled by the instruction. Figure D.1 (on the next page) shows these register paths. The 1-bit Bypass register is fully defined in the 1149.1 specification. The Boundary register is described in the next section.

No special values need be written into any register prior to selection of any instruction. As Table D.1 shows, certain instructions are reserved for emulator use. See Section D.7 for more information.

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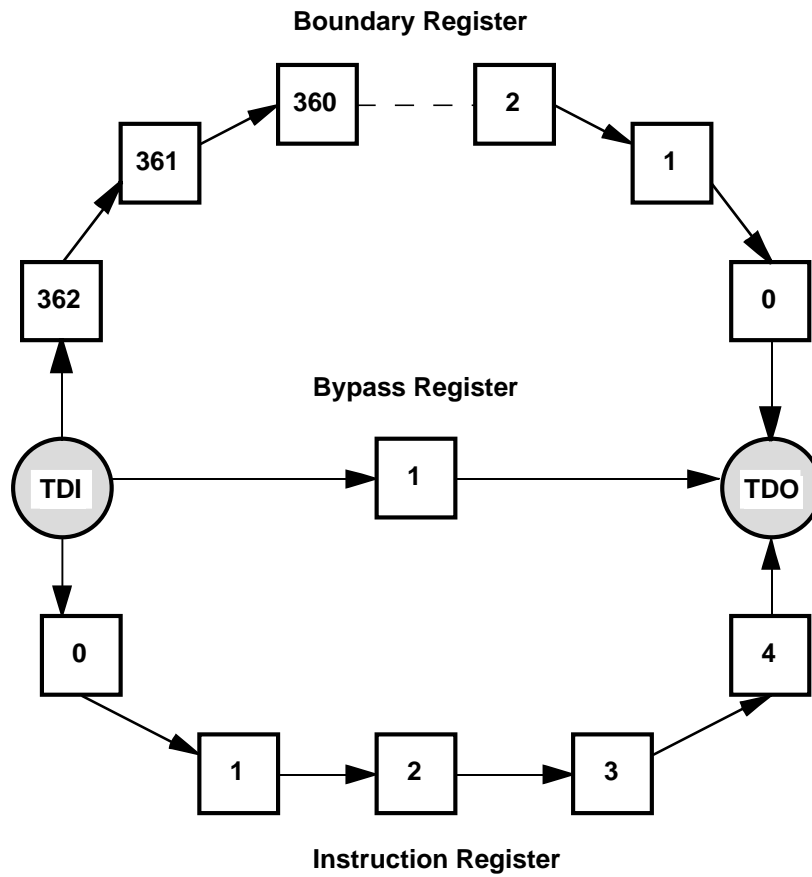


Figure D.1 Serial Scan Paths

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D.4 BOUNDARY REGISTER

The Boundary register is 363 bits long. This section defines the latch type and function of each position in the scan path. The positions are numbered with 0 being the first bit output (closest to TDO) and 362 being the last (closest to TDI).

<u>Scan Position</u>	<u>Latch Type</u>	<u>Signal Name</u>	
0	input	$\overline{\text{IRQ0}}$	<i>this end closest to TDO (scan in first)</i>
1	input	$\overline{\text{IRQ1}}$	
2	input	$\overline{\text{IRQ2}}$	
3	input	EBOOT	
4	input	$\overline{\text{RESET}}$	
5	input	RPBA	
6	input	LBOOT	
7	input	IDO	
8	input	ID1	
9	input	ID2	
10	output	L5ACK (NC on the ADSP-21061)	
11	input	L5ACK (NC on the ADSP-21061)	
12	output	L5CLK (NC on the ADSP-21061)	
13	input	L5CLK (NC on the ADSP-21061)	
14	output	L5DAT0 (NC on the ADSP-21061)	
15	input	L5DAT0 (NC on the ADSP-21061)	
16	output	L5DAT1 (NC on the ADSP-21061)	
17	input	L5DAT1 (NC on the ADSP-21061)	
18	output	L5DAT2 (NC on the ADSP-21061)	
19	input	L5DAT2 (NC on the ADSP-21061)	
20	output	L5DAT3 (NC on the ADSP-21061)	
21	input	L5DAT3 (NC on the ADSP-21061)	
22	output enable	L5ACK output enable (NC on the ADSP-21061)	
23	output enable	L5DATx, L5CLK output enable (NC on the ADSP-21061)	
24	output	L4ACK (NC on the ADSP-21061)	
25	input	L4ACK (NC on the ADSP-21061)	
26	output	L4CLK (NC on the ADSP-21061)	
27	input	L4CLK (NC on the ADSP-21061)	
28	output	L4DAT0 (NC on the ADSP-21061)	
29	input	L4DAT0 (NC on the ADSP-21061)	
30	output	L4DAT1 (NC on the ADSP-21061)	
31	input	L4DAT1 (NC on the ADSP-21061)	
32	output	L4DAT2 (NC on the ADSP-21061)	
33	input	L4DAT2 (NC on the ADSP-21061)	
34	output	L4DAT3 (NC on the ADSP-21061)	
35	input	L4DAT3 (NC on the ADSP-21061)	
36	output enable	L4ACK output enable (NC on the ADSP-21061)	
37	output enable	L4DATx, L4CLK output enable (NC on the ADSP-21061)	
38	output	L3ACK (NC on the ADSP-21061)	
39	input	L3ACK (NC on the ADSP-21061)	

Output Enables:

- 1 = Drive the associated signals during the EXTEST and INTEST instructions
- 0 = Tristate the associated signals during the EXTEST and INTEST instructions

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<u>Scan Position</u>	<u>Latch Type</u>	<u>Signal Name</u>
40	output	L3CLK (NC on the ADSP-21061)
41	input	L3CLK (NC on the ADSP-21061)
42	output	L3DAT0 (NC on the ADSP-21061)
43	input	L3DAT0 (NC on the ADSP-21061)
44	output	L3DAT1 (NC on the ADSP-21061)
45	input	L3DAT1 (NC on the ADSP-21061)
46	output	L3DAT2 (NC on the ADSP-21061)
47	input	L3DAT2 (NC on the ADSP-21061)
48	output	L3DAT3 (NC on the ADSP-21061)
49	input	L3DAT3 (NC on the ADSP-21061)
50	output enable	L3ACK output enable (NC on the ADSP-21061)
51	output enable	L3DATx, L3CLK output enable (NC on the ADSP-21061)
52	output	NC (Do Not Connect)
53	input	NC (Do Not Connect)
54	output	L2ACK (NC on the ADSP-21061)
55	input	L2ACK (NC on the ADSP-21061)
56	output	L2CLK (NC on the ADSP-21061)
57	input	L2CLK (NC on the ADSP-21061)
58	output	L2DAT0 (NC on the ADSP-21061)
59	input	L2DAT0 (NC on the ADSP-21061)
60	output	L2DAT1 (NC on the ADSP-21061)
61	input	L2DAT1 (NC on the ADSP-21061)
62	output	L2DAT2 (NC on the ADSP-21061)
63	input	L2DAT2 (NC on the ADSP-21061)
64	output	L2DAT3 (NC on the ADSP-21061)
65	input	L2DAT3 (NC on the ADSP-21061)
66	output enable	L2ACK output enable (NC on the ADSP-21061)
67	output enable	L2DATx, L2CLK output enable (NC on the ADSP-21061)
68	output	L1ACK (NC on the ADSP-21061)
69	input	L1ACK (NC on the ADSP-21061)
70	output	L1CLK (NC on the ADSP-21061)
71	input	L1CLK (NC on the ADSP-21061)
72	output	L1DAT0 (NC on the ADSP-21061)
73	input	L1DAT0 (NC on the ADSP-21061)
74	output	L1DAT1 (NC on the ADSP-21061)
75	input	L1DAT1 (NC on the ADSP-21061)
76	output	L1DAT2 (NC on the ADSP-21061)
77	input	L1DAT2 (NC on the ADSP-21061)
78	output	L1DAT3 (NC on the ADSP-21061)
79	input	L1DAT3 (NC on the ADSP-21061)
80	output enable	L1ACK output enable (NC on the ADSP-21061)
81	output enable	L1DATx, L1CLK output enable (NC on the ADSP-21061)
82	output	L0ACK (NC on the ADSP-21061)
83	input	L0ACK (NC on the ADSP-21061)
84	output	L0CLK (NC on the ADSP-21061)
85	input	L0CLK (NC on the ADSP-21061)
86	output	L0DAT0 (NC on the ADSP-21061)
87	input	L0DAT0 (NC on the ADSP-21061)
88	output	L0DAT1 (NC on the ADSP-21061)
89	input	L0DAT1 (NC on the ADSP-21061)

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<u>Scan Position</u>	<u>Latch Type</u>	<u>Signal Name</u>
90	output	L0DAT2 (NC on the ADSP-21061)
91	input	L0DAT2 (NC on the ADSP-21061)
92	output	L0DAT3 (NC on the ADSP-21061)
93	input	L0DAT3 (NC on the ADSP-21061)
94	output enable	L0ACK output enable (NC on the ADSP-21061)
95	output enable	L0DATx, L0CLK output enable (NC on the ADSP-21061)
96	output	DATA0
97	input	DATA0
98	output	DATA1
99	input	DATA1
100	output	DATA2
101	input	DATA2
102	output	DATA3
103	input	DATA3
104	output	DATA4
105	input	DATA4
106	output	DATA5
107	input	DATA5
108	output	DATA6
109	input	DATA6
110	output	DATA7
111	input	DATA7
112	output	DATA8
113	input	DATA8
114	output	DATA9
115	input	DATA9
116	output	DATA10
117	input	DATA10
118	output	DATA11
119	input	DATA11
120	output	DATA12
121	input	DATA12
122	output	DATA13
123	input	DATA13
124	output	DATA14
125	input	DATA14
126	output	DATA15
127	input	DATA15
128	output	DATA16
129	input	DATA16
130	output	DATA17
131	input	DATA17
132	output	DATA18
133	input	DATA18
134	output	DATA19
135	input	DATA19
136	output	DATA20
137	input	DATA20
138	output	DATA21
139	input	DATA21

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<u>Scan Position</u>	<u>Latch Type</u>	<u>Signal Name</u>
140	output	DATA22
141	input	DATA22
142	output	DATA23
143	input	DATA23
144	output	DATA24
145	input	DATA24
146	output	DATA25
147	input	DATA25
148	output	DATA26
149	input	DATA26
150	output enable	DATAx output enable
151	output	DATA27
152	input	DATA27
153	output	DATA28
154	input	DATA28
155	output	DATA29
156	input	DATA29
157	output	DATA30
158	input	DATA30
159	output	DATA31
160	input	DATA31
161	output	DATA32
162	input	DATA32
163	output	DATA33
164	input	DATA33
165	output	DATA34
166	input	DATA34
167	output	DATA35
168	input	DATA35
169	output	NC (Do Not Connect)
170	input	NC (Do Not Connect)
171	output	DATA36
172	input	DATA36
173	output	DATA37
174	input	DATA37
175	output	DATA38
176	input	DATA38
177	output	DATA39
178	input	DATA39
179	output	DATA40
180	input	DATA40
181	output	DATA41
182	input	DATA41
183	output	DATA42
184	input	DATA42
185	output	DATA43
186	input	DATA43
187	output	DATA44
188	input	DATA44
189	output	DATA45

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<u>Scan Position</u>	<u>Latch Type</u>	<u>Signal Name</u>
190	input	DATA45
191	output	DATA46
192	input	DATA46
193	output	DATA47
194	input	DATA47
195	output enable	BR1 output enable
196	output enable	BR2 output enable
197	output enable	BR3 output enable
198	output	BR1
199	input	BR1
200	output	BR2
201	input	BR2
202	output	BR3
203	input	BR3
204	output	BR4
205	input	BR4
206	output	BR5
207	input	BR5
208	output	BR6
209	input	BR6
210	output enable	BR4 output enable
211	output enable	BR5 output enable
212	output enable	BR6 output enable
213	output	PAGE
214	input	PAGE
215	output	DMAG1
216	output	DMAG2
217	output	ACK
218	input	ACK
219	clock*	CLKIN
220	output enable	ACK output enable
221	output enable	RD, WR, PAGE, ADRCLK, $\overline{\text{DMAGx}}$ output enable
222	output	WR
223	input	WR
224	output	RD
225	input	RD
226	input	$\overline{\text{CS}}$
227	output	HBG
228	input	HBG
229	output	REDY
230	output	ADRCLK
231	output enable	HBG output enable
232	output enable	REDY output enable
233	output enable	RFS0 output enable
234	output enable	RCLK0 output enable
235	output enable	TFS0 output enable
236	output enable	TCLK0 output enable
237	output enable	DT0 output enable
238	output	RFS0
239	input	RFS0

* CLKIN can be sampled but not controlled (read-only). CLKIN continues to clock the ADSP-2106x no matter which instruction is enabled.

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<u>Scan Position</u>	<u>Latch Type</u>	<u>Signal Name</u>
240	output	RCLK0
241	input	RCLK0
242	input	DR0
243	output	TFS0
244	input	TFS0
245	output	TCLK0
246	input	TCLK0
247	output	DT0
248	output	\overline{CPA}
249	input	CPA
250	output enable	RFS1, \overline{CPA} output enable
251	output enable	RCLK1 output enable
252	output enable	TFS1 output enable
253	output enable	TCLK1 output enable
254	output enable	DT1 output enable
255	output	RFS1
256	input	RFS1
257	output	RCLK1
258	input	RCLK1
259	input	DR1
260	output	TFS1
261	input	TFS1
262	output	TCLK1
263	input	TCLK1
264	output	DT1
265	input	HBR
266	input	DMAR1
267	input	DMAR2
268	input	SBTS
269	output	ADDR31
270	input	ADDR31
271	output	ADDR30
272	input	ADDR30
273	output	ADDR29
274	input	ADDR29
275	output enable	BMS output enable
276	output	ADDR28
277	input	ADDR28
278	output	\overline{BMS}
279	input	BMS
280	output	\overline{SW}
281	input	SW
282	output	$\overline{MS0}$
283	input	MS0
284	output	$\overline{MS1}$
285	input	MS1
286	output	$\overline{MS2}$
287	input	MS2
288	output	$\overline{MS3}$
289	input	MS3

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<u>Scan Position</u>	<u>Latch Type</u>	<u>Signal Name</u>
290	output	ADDR27
291	input	ADDR27
292	output	ADDR26
293	input	ADDR26
294	output	ADDR25
295	input	ADDR25
296	output	ADDR24
297	input	ADDR24
298	output	ADDR23
299	input	ADDR23
300	output	ADDR22
301	input	ADDR22
302	output	ADDR21
303	input	ADDR21
304	output	ADDR20
305	input	ADDR20
306	output	ADDR19
307	input	ADDR19
308	output enable	ADDRx, MSx, SW output enable
309	output	ADDR18
310	input	ADDR18
311	output	ADDR17
312	input	ADDR17
313	output	ADDR16
314	input	ADDR16
315	output	ADDR15
316	input	ADDR15
317	output	ADDR14
318	input	ADDR14
319	output	ADDR13
320	input	ADDR13
321	output	ADDR12
322	input	ADDR12
323	output	ADDR11
324	input	ADDR11
325	output	ADDR10
326	input	ADDR10
327	output	ADDR9
328	input	ADDR9
329	output	ADDR8
330	input	ADDR8
331	output	ADDR7
332	input	ADDR7
333	output	ADDR6
334	input	ADDR6
335	output	ADDR5
336	input	ADDR5
337	output	ADDR4
338	input	ADDR4
339	output	ADDR3

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<u>Scan Position</u>	<u>Latch Type</u>	<u>Signal Name</u>	
340	input	ADDR3	
341	output	ADDR2	
342	input	ADDR2	
343	output	ADDR1	
344	input	ADDR1	
345	output	ADDR0	
346	input	ADDR0	
347	output enable	FLAG0 output enable	
348	output enable	FLAG1 output enable	
349	output enable	FLAG2 output enable	
350	output enable	FLAG3 output enable	
351	output	FLAG0	
352	input	FLAG0	
353	output	FLAG1	
354	input	FLAG1	
355	output	FLAG2	
356	input	FLAG2	
357	output	FLAG3	
358	input	FLAG3	
359	output	ICSA	
360	output	EMU	
361	output	TIMEXP	
362	output enable	EMU output enable	<i>this end closest to TDI (scan in last)</i>

Output Enables:

- 1 = Drive the associated signals during the EXTEST and INTEST instructions
- 0 = Tristate the associated signals during the EXTEST and INTEST instructions

JTAG Test Access Port D

D.5 DEVICE IDENTIFICATION REGISTER

No device identification register is included in the ADSP-2106x.

D.6 BUILT-IN SELF-TEST OPERATION (BIST)

No self-test functions are supported by the ADSP-2106x.

D.7 PRIVATE INSTRUCTIONS

Loading a value of 001xx into the instruction register enables the private instructions reserved for emulation. The ADSP-2106x EZ-ICE emulator uses the TAP and boundary scan as a way to access the processor in the target system. The EZ-ICE emulator requires a target board connector for access to the TAP. See “EZ-ICE Emulator” in Chapter 11, *System Design*, for information on this connector.

D.8 REFERENCES

IEEE Standard 1149.1-1990. *Standard Test Access Port and Boundary-Scan Architecture*. To order a copy, contact IEEE at 1-800-678-IEEE.

Maunder, C.M. & R. Tulloss. *Test Access Ports and Boundary Scan Architectures*. IEEE Computer Society Press, 1991.

Parker, Kenneth. *The Boundary Scan Handbook*. Kluwer Academic Press, 1992.

Bleeker, Harry, P. van den Eijnden, & F. de Jong. *Boundary-Scan Test—A Practical Approach*. Kluwer Academic Press, 1993.

Hewlett-Packard Co. *HP Boundary-Scan Tutorial and BSDL Reference Guide*. (HP part# E1017-90001.) 1992.

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